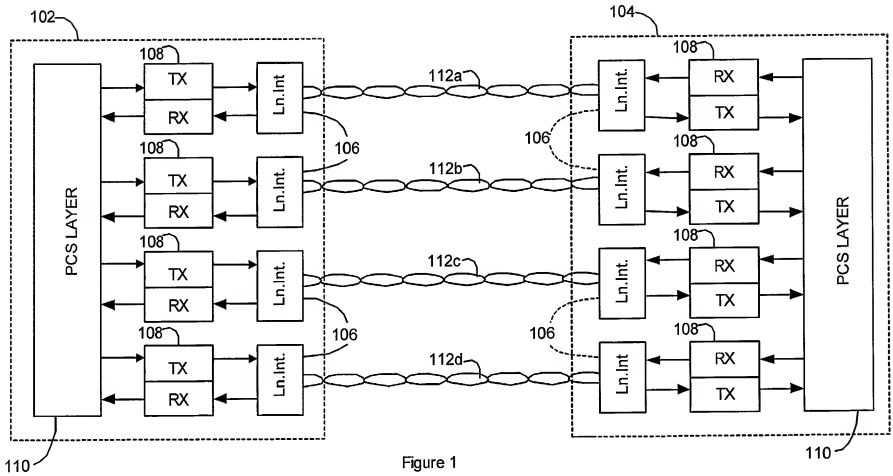


Figure 1

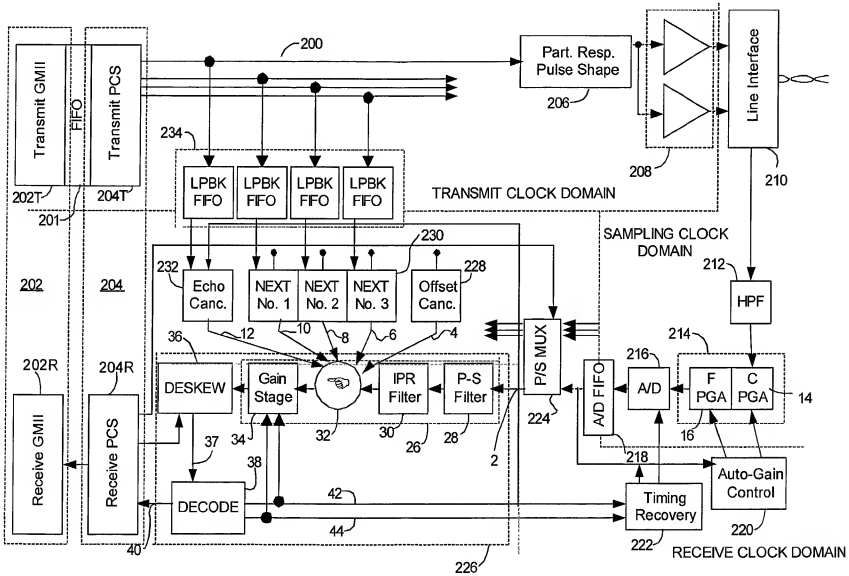

Transmit GMII
FIFO
Transmit PCS
200
Part. Resp. Pulse Shape
206
Line Interface
208
210
234
LPBK FIFO
LPBK FIFO
LPBK FIFO
LPBK FIFO
TRANSMIT CLOCK DOMAIN
202T
201
204T
SAMPLING CLOCK DOMAIN
230
232
Echo Canc.
NEXT No. 1
NEXT No. 2
NEXT No. 3
Offset Canc.
228
212
HPF
202
204
36
12
10
8
6
4
214
216
202R
204R
DESKEW
Gain Stage
IPR Filter
P-S Filter
P/S MUX
A/D FIFO
A/D
F PGA
C PGA
14
16
Receive GMII
Receive PCS
37
34
32
30
26
28
2
224
218
38
Auto-Gain Control
DECODE
42
Timing Recovery
44
220
222
40
226
RECEIVE CLOCK DOMAIN

Figure 2

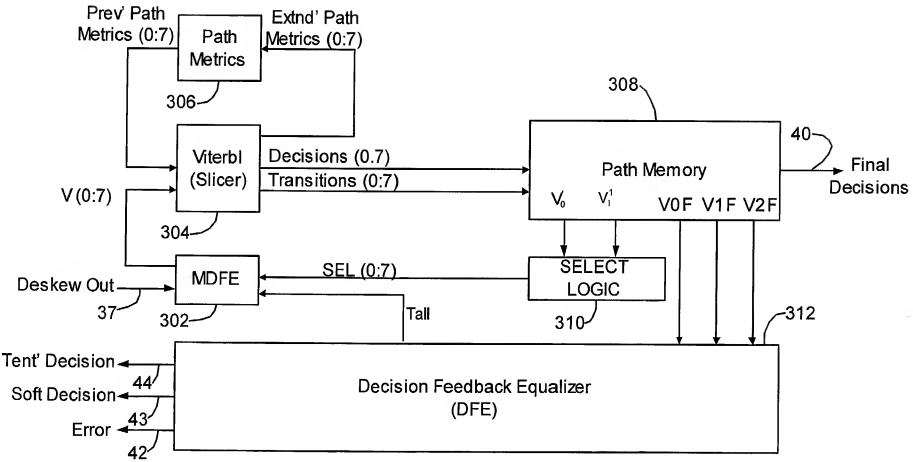

Prev' Path Metrics (0:7)
Path Metrics
Extnd' Path Metrics (0:7)
306
308
40
Viterbi (Slicer)
Decisions (0.7)
Transitions (0:7)
Path Memory
Final Decisions
V(0:7)
V_0
V_1
V0F V1F V2F
304
Deskew Out
MDFE
SEL (0:7)
SELECT LOGIC
37
302
Tall
310
312
Tent' Decision
44
Soft Decision
43
Error
42
Decision Feedback Equalizer (DFE)

Figure 3

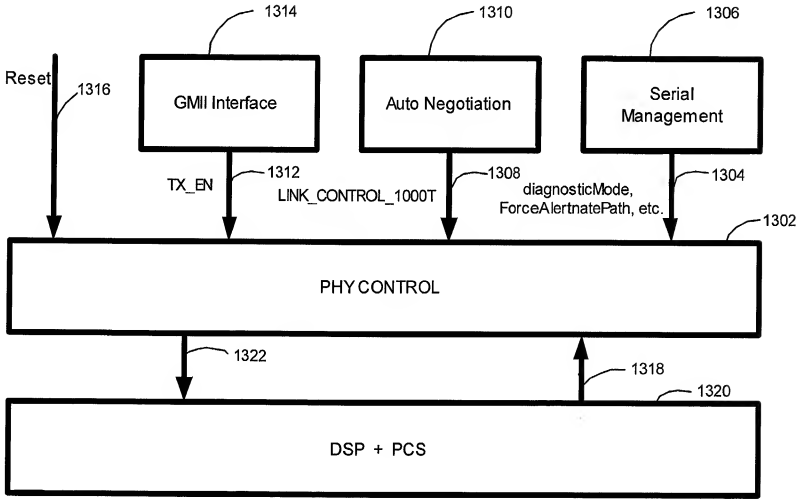

1314
1310
1306
Reset
1316
GMII Interface
Auto Negotiation
Serial Management
TX_EN
1312
LINK_CONTROL_1000T
1308
diagnosticMode,
ForceAlertnatePath, etc.
1304
1302
PHY CONTROL
1322
1318
1320
DSP + PCS

FIG. 4

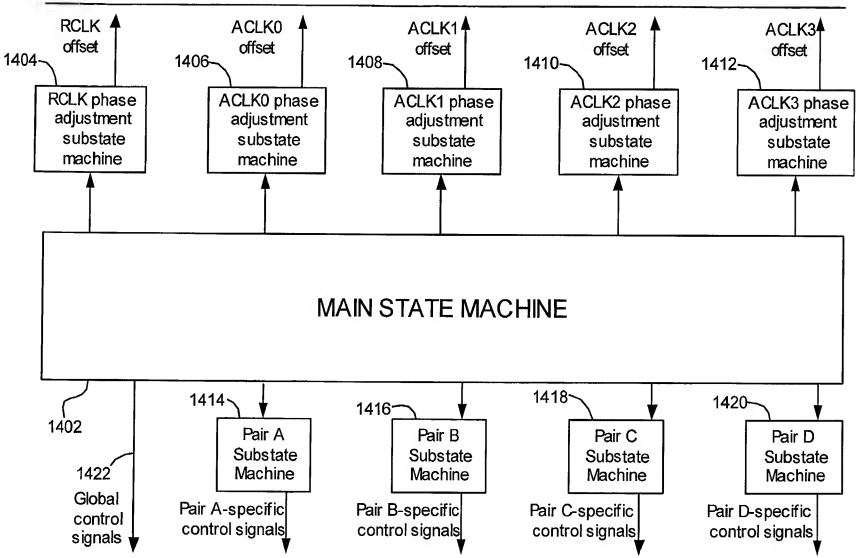

RCLK offset
1404
RCLK phase adjustment substate machine
ACLK0 offset
1406
ACLK0 phase adjustment substate machine
ACLK1 offset
1408
ACLK1 phase adjustment substate machine
ACLK2 offset
1410
ACLK2 phase adjustment substate machine
ACLK3 offset
1412
ACLK3 phase adjustment substate machine
MAIN STATE MACHINE
1402
1422
Global control signals
1414
Pair A Substate Machine
Pair A-specific control signals
1416
Pair B Substate Machine
Pair B-specific control signals
1418
Pair C Substate Machine
Pair C-specific control signals
1420
Pair D Substate Machine
Pair D-specific control signals

Figure 5

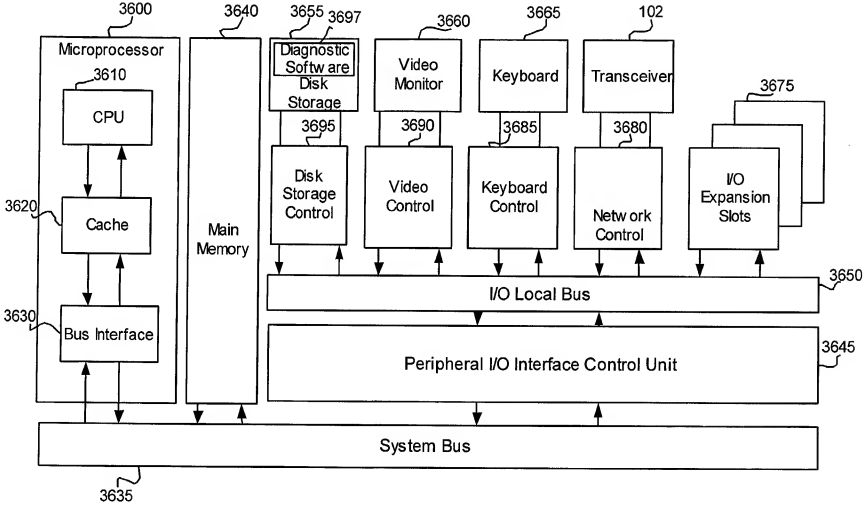

3600
Microprocessor
3610
CPU
3620
Cache
3630
Bus Interface
3640
Main Memory
3655
3697
Diagnostic Software
Disk Storage
3695
Disk Storage Control
3660
Video Monitor
3690
Video Control
3665
Keyboard
3685
Keyboard Control
102
Transceiver
3680
Network Control
3675
I/O Expansion Slots
3650
I/O Local Bus
3645
Peripheral I/O Interface Control Unit
System Bus
3635

Figure 6

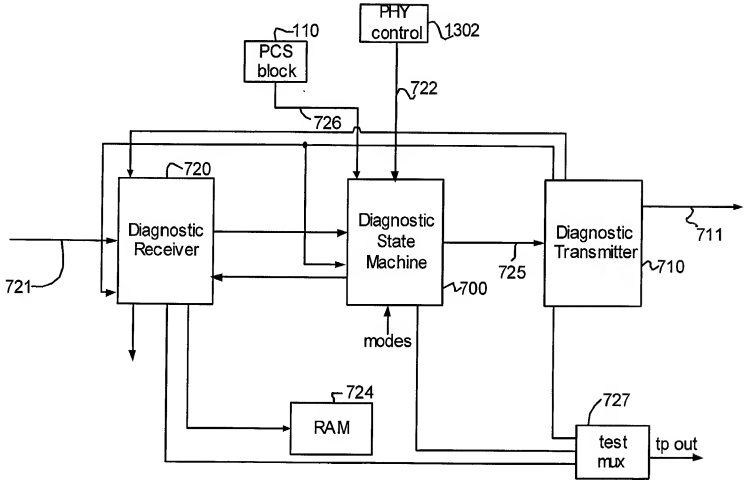

PHY control
1302
110
PCS block
722
726
720
Diagnostic Receiver
Diagnostic State Machine
Diagnostic Transmitter
711
721
725
710
700
modes
724
RAM
727
test mux
tp out

Figure 7

Master - no FEXT

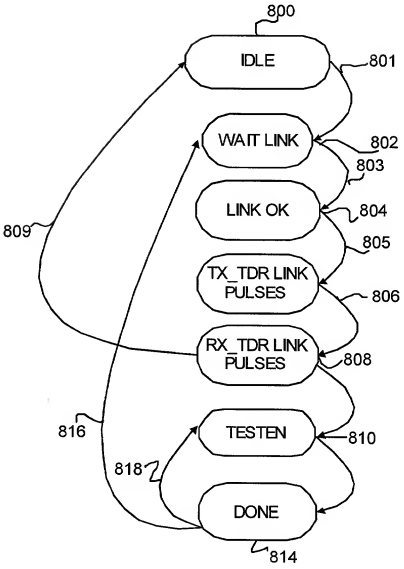


Figure 8

slave - no FEXT

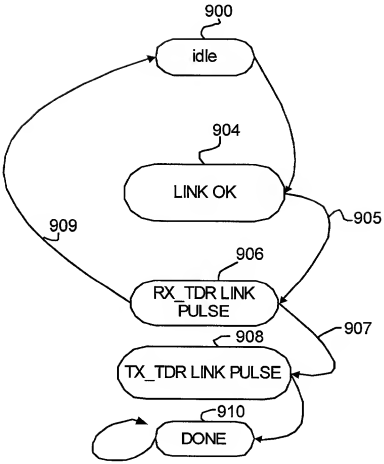


Figure 9

Echo/Next - no extphy

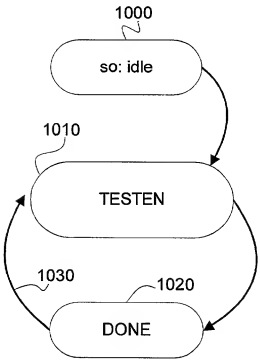


Figure 10

Master - FEXT

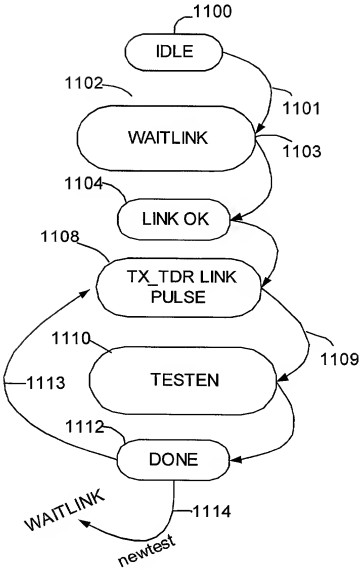


Figure 11

Slave- fext

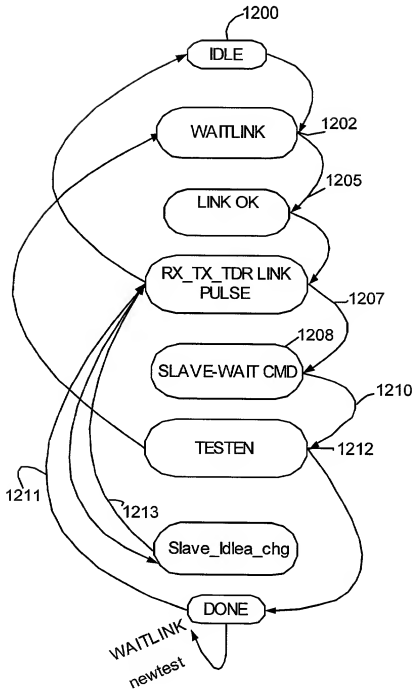


Figure 12

linkdet fsm

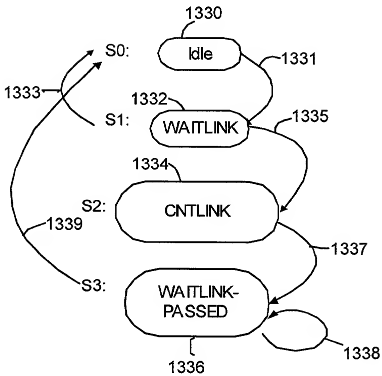
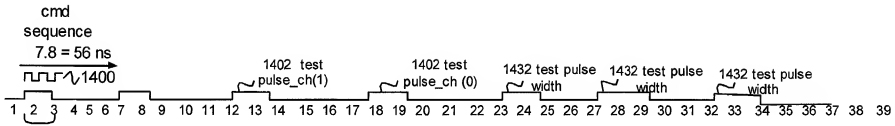


Figure 13

FEXT: and signaling



max # times asserted = 3 T cycles

min # times asserted = 2 T cycles

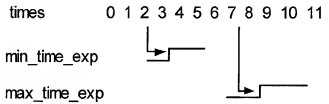


Figure 14

LINKPULSE/TEST PULSE TIMING - NO FEXT

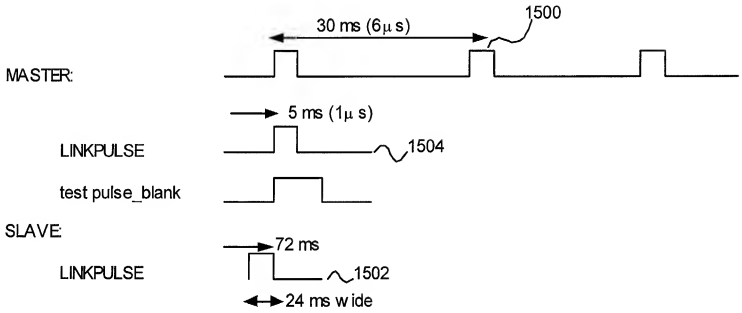


Figure 15

MDIX: Link pulse - no fext

1) No mdix

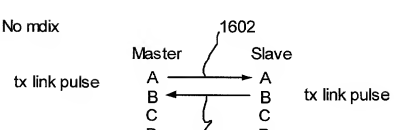


Figure 16A

2) mdix

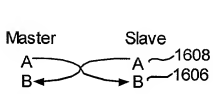


Figure 16B

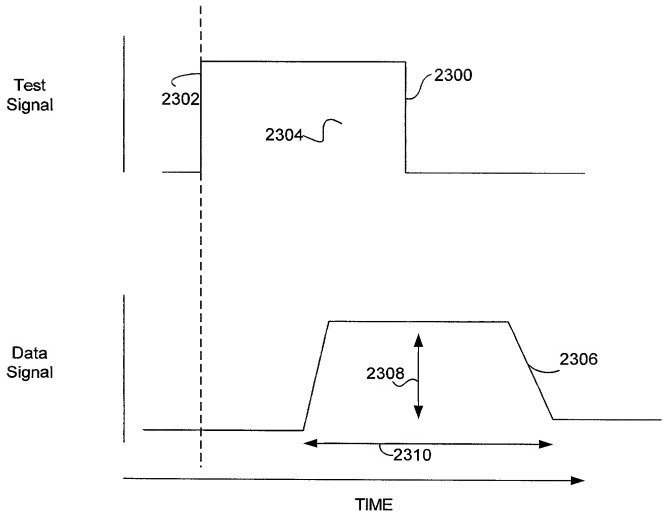


Figure 17

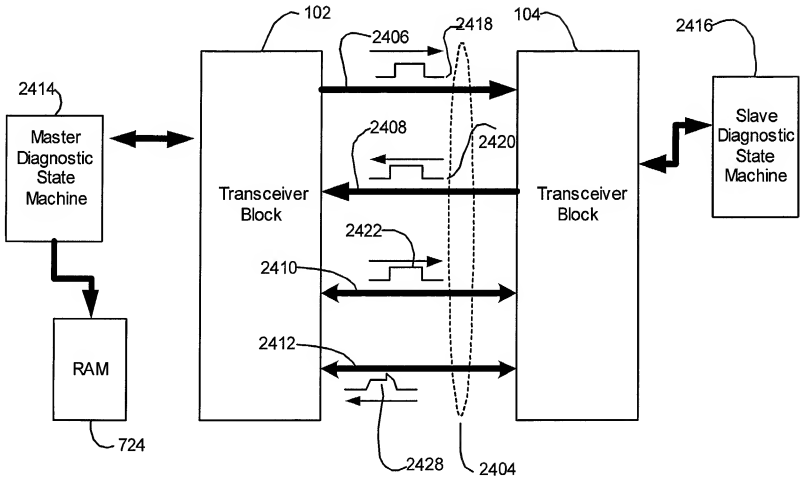

102
104
2406
2418
2416
2414
Master Diagnostic State Machine
2408
2420
Transceiver Block
Transceiver Block
Slave Diagnostic State Machine
2422
2410
2412
RAM
724
2428
2404

Figure 18

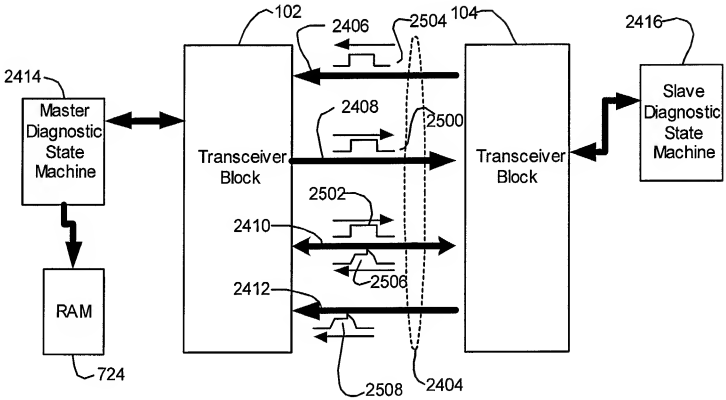


Figure 19

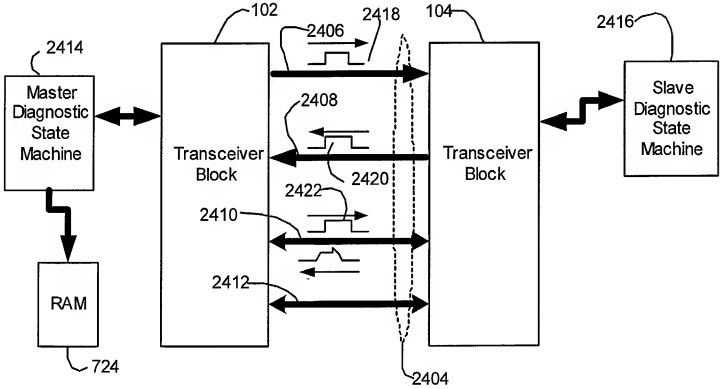

102
2418
104
2416
2406
2414
Master Diagnostic State Machine
2408
Transceiver Block
2420
Transceiver Block
Slave Diagnostic State Machine
2422
2410
2412
RAM
724
2404

Figure 20